Optimum Design of an Envelope Tracking Buck Converter for RFPA using GaN HEMTs

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***Abstract*—In this paper, filter design methodology and application of GaN HEMTs for high efficiency Envelope Amplifier in RF transmitters are proposed. The main objectives of the filter design are generation of the envelope reference with the minimum possible distortion and high efficiency of the amplifier obtained by the optimum trade–off between conduction and switching losses. This optimum point was determined using power losses model for synchronous buck with sinusoidal output voltage and experimental results showed good correspondence with the model and verified the proposed methodology. On the other hand, comparing to Si MOSFETs, GaN HEMTs can provide higher efficiency of the envelope amplifier, due to superior conductivity and switching characteristics. Experimental results verified benefits of GaN devices comparing to the appliance of Si switching devices with very good Figure Of Merit, for this particular application.**

I. INTRODUCTION

In the modern world of communications today, the demand for broadband and wireless services is growing on a daily basis. The direct consequence of this development is the growth of the networks that have to provide these services and one of the problems is their energy consumption. The main reasons for the low efficiency of the radio base stations is poor efficiency of linear power amplifiers, employed to transmit the signal. There are a lot of techniques that are used in order to enhance the efficiency of Radio Frequency Power Amplifier, but two of them are mostly exploited lately: Envelope Tracking (ET) [1] and Kahn's Technique or Envelope Elimination and Restoration (EER) Technique, presented in Figure 1 [2]. Both techniques are based on the voltage modulation at the output of the power supply for RFPA. The converter that supplies the energy is the Envelope Amplifier.

The Envelope Amplifier in EER should have fast dynamic response, high efficiency and minimal interference with the output spectrum of the transmitter. A Synchronous Buck converter which can be used for this purpose, needs to fulfill the following requirements: reference tracking of modulating voltage, high linearity, low phase delay, high efficiency. The bandwidth of the converter, the ripple of the output voltage and the converter's efficiency depend on the selection of the switching frequency and the design of the output filter.

This work has been supported by the Ministry of Education and Science of Spain for the projects TEC2009-14307-C02-01 and CSD 2009 - 00046

In order to obtain high bandwidth, very high switching frequency is needed. This usually implies high switching losses and low efficiency of the converter.

Another important issue is the additional spectral components of the converter output voltage, created by the modulation of the duty cycle in order to reproduce the desired envelope. These spectral components are around the converter's switching frequency and its multiples.

In order to obtain high efficiency of the converter operating at high switching frequencies, we need transistors with good Figure Of Merit (product of on-resistance and gate charge). New generation of Enhancement mode HEMTs built with Gallium Nitride on Silicon, presents a good replacement for Silicon power MOSFETs, because of promising conductivity and switching characteristics of GaN devices [3], [4], [5], [6], [7].

There are two main objectives of this paper: the first one is to present the methodology for filter design in synchronous buck for RF PA and the second one is to show the advantages of GaN HEMTs comparing to Si MOSFETs.

II. OUTPUT FILTER DESIGN

The main objectives of the filter design in synchronous buck for RF PA are generation of the envelope reference with minimum possible distortion and high efficiency of the converter obtained by the optimum trade-off between conduction and switching losses.

Regarding the selection of a correct switching frequency, an analysis of the inter-modulation products induced by the PWM on the envelope signal is an important issue. It is assumed that the modulating signal with tone frequency f_{mod} yields duty cycle d(t) in the power stage [7]

$$d(t) = \frac{\alpha}{2}(1 + \sin(2\pi f_{mod} t)) \quad (1)$$

A single tone modulating signal is used to establish the Fourier series decomposition of the PWM signal at the input of the filter, using the Bessels functions of the first kind [7]. For a multi-tone like RF envelope, the analysis is very difficult though [8] proposes a method to determine an equivalent single tone. The PWM spectrum for a single tone modulation shows that no harmonics contribution of f_{mod} is present in the spectrum and most of the additional spectral components are concentrated in high frequency range, around the harmonics of

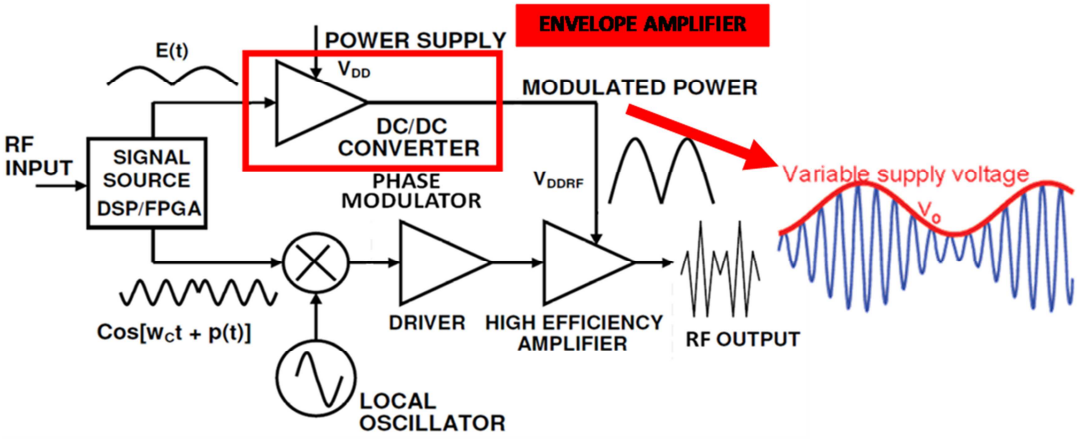

Fig. 1 Block Scheme of Kahn Technique Transmitter

the switching frequency [7]. In order to minimize the high frequency components, the switching frequency should be increased so that corresponding spurious frequencies fall in the frequency range where the attenuation of the LC output filter is high enough.

In order to obtain the desired attenuation of the duty cycle to output voltage transfer function for the filter with resonance frequency equal to f_0, the minimum switching frequency, f_{sw}, is defined as

$$f_{sw} = f_0 \, 10^{\frac{a_{tt}}{40}} \tag{2}$$

where a_{tt} is a desired attenuation in dB (Figure 3). The resonance frequency of the filter is given by

$$f_0 = \frac{1}{2\pi\sqrt{L_{OUT}C_{OUT}}} \tag{3}$$

where C_{OUT} and L_{OUT} are the values for the filter inductor and capacitor which provide optimum trade-off between conduction and switching losses.

In order to achieve that, it is necessary to minimize the conduction losses

$$P_{MOS} = R_{DSON} \, {I_{L\_RMS}}^2 \tag{4a}$$

$$P_L = R_L {I_{L\_RMS}}^2 \tag{4b}$$

$$P_C = R_{ESR} \, {I_{C\_RMS}}^2 \tag{4c}$$

as well as switching losses, which will be presented in the next section. In the previous equations, I_{L_RMS} and I_{C_RMS} are the RMS values of the inductor and capacitor current while R_{DSON}, R_L and R_{ESR} present the on resistance of the switch, resistance of the inductor and equivalent series resistance of the capacitor, respectively.

Analyzing the circuit from Figure 2, we obtain that the inductor to load current ratio is given by

$$\frac{i_L}{i_{LOAD}} = 1 + R_{LOAD} C_{OUT} \, s \tag{5}$$

and its frequency dependence is presented in Figure 4. If we select the frequency equal to the frequency of the output modulated voltage, from (5) we obtain

$$\frac{i_{Lmax}}{i_{LOADmax}} (j2\pi f_{MOD}) = A \tag{6}$$

where A is the design parameter which always complies the condition:

$$A \geq 1 \tag{7}$$

and i_{LMAX}, $i_{LOADMAX}$ are the maximum values of the inductor and load current, respectively. Assuming that the ratio of these maximum values is set to A, for C_{OUT} we obtain

$$C_{OUT} = \frac{\sqrt{A^2 - 1}}{2\pi f_{MOD} R_{LOAD}} \tag{8}$$

Higher values for C_{OUT} correspond to higher values of A and higher conduction losses. Minimization of C_{OUT} provides lower conduction losses but increases a corner frequency of the filter. This implies the higher switching frequency for the same attenuation value and higher switching losses. In order to decrease the corner frequency of the filter, we choose the maximum value for the inductance L_{OUT}.

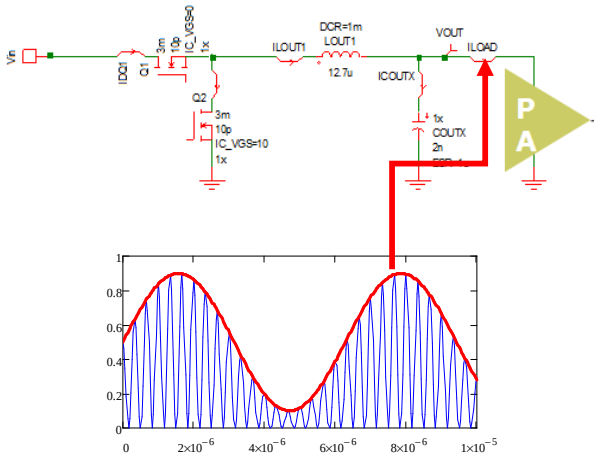

Fig. 2 Synchronous Buck for RF PA

The criteria for L_{OUT} determination is to avoid duty cycle saturation. From $G_{vd}(s)$ we obtain

$$d(s) = {G_{vd}}^{-1}(s) v_{OUT}(s) \tag{9}$$

where $d(s)$ (Figure 5) and $v_{OUT}(s)$ present the duty cycle and the output voltage in the frequency domain.

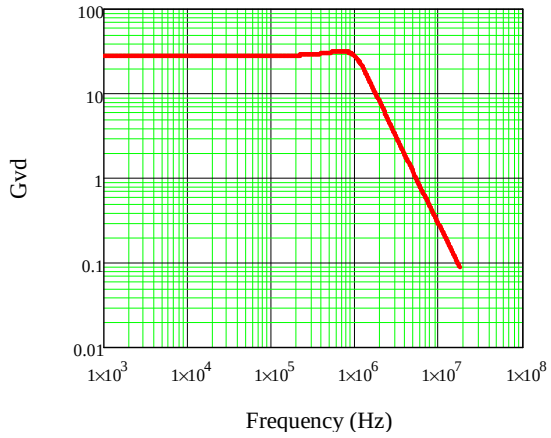

Fig. 3 Duty cycle to output voltage transfer function

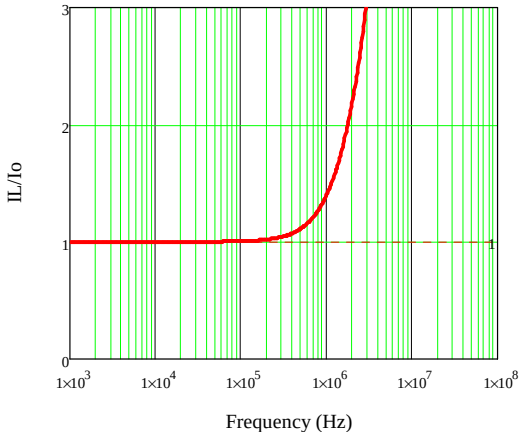

Fig. 4. Frequency dependence of inductor to load current ratio

If the maximum change of the output voltage equal to Δv_{OUT} corresponds to the maximum change of the duty cycle, Δd=1, we obtain

$$\frac{\Delta v_{OUT}}{V_{IN}} \sqrt{[1 - L_{OUT}C_{OUT}(2\pi f_{MOD})^2]^2 + \frac{L_{OUT}}{R_{LOAD}}(2\pi f_{MOD})^2} = 1 \quad (10)$$

where V_{IN} is the input voltage of the converter. Solving the previous equation we obtain the value for $L_{OUT.}$

In order to determine the total losses dependence on the filter design parameter A, the switching losses model is determined [9]. The difference comparing to the model developed in [9] is the assumption that output voltage is sinusoidal, which affects the model equations. Equations (11), (12) and (13) for the high-side switching losses, contain the average value of the inductor current, instead of the load current that was used in [9]. The same approach is applied for low-side switching losses.

The switching interval begins when the high-side driver turns on and starts to supply current to high-side gate to charge its input capacitance. There are no switching losses until V_{GS} reaches the threshold voltage, V_{TH}. Therefore, losses during this time interval are zero.

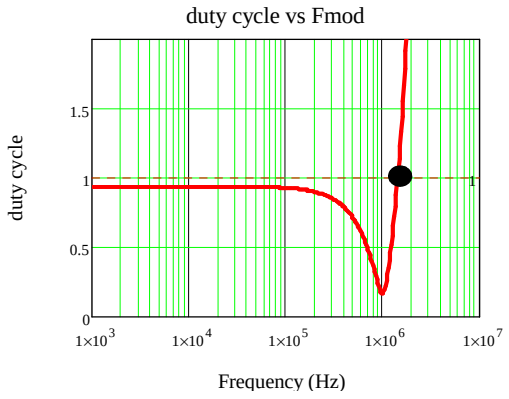

Fig. 5. Frequency dependence of the duty cycle

When V_{GS} reaches V_{TH}, the input capacitance C_{ISS} is being charged and the drain current is rising linearly until it reaches the inductor current. During this time interval, t_2, the switch is sustaining the entire input voltage across it. The energy in the high-side transistor during t_2 is:

$$E_{t2} = t_2\left(\frac{V_{IN}I_{LAVG}}{2}\right) \quad (11)$$

where I_{LAVG} is the average value of inductor current.

When the next time interval, t_3, starts, all of the gate current will be going to recharge the capacitance between gate and drain, C_{GD}, and V_{DS} begins to fall from V_{IN} to zero. Therefore:

$$E_{t3} = t_3\left(\frac{V_{IN}I_{LAVG}}{2}\right) \quad (12)$$

From (11) and (12), for the main part of high-side switching losses we obtain:

$$P_{sw\_hs} = \left(\frac{V_{IN}I_{LAVG}}{2}\right)(t_2 + t_3)\, f_{sw} \quad (13)$$

Time intervals t_2 and t_3 are determined by the driver capability to deliver all of the charge required in that time period. Detailed analysis and mathematical expressions for t_2 and t_3 are provided in [9].

Low-side switching losses can be calculated in a similar way [9].

In addition to aforementioned, there are losses that are typically much smaller but should be taken into consideration. The first among them are gate losses of the switch

$$P_{GATE} = Q_{GATE}\, V_{DD}\, f_{SW} \quad (14)$$

where Q_{GATE} is the gate charge of the switching device, V_{DD} is the supply voltage of the driver and f_{SW} is the switching frequency.

The second one is the power to charge the output capacitance of the switch

$$P_{COSS} \approx \frac{V_{IN}^2\, f_{SW} C_{OSS}}{2} \quad (15)$$

From the previously calculated expressions for power losses, we obtain the approximate model for the total power losses.

If we implement the power losses model in Matlab, we obtain the losses dependence on the filter design parameter A. The mean value of the inductor current was calculated using the number of samples which is equal to the ratio of the switching frequency and frequency of the output voltage, f_{SW}/f_{MOD}. Figure 6 presents the efficiency dependence of a synchronous buck converter on the filter parameter A. The results from Figure 6 are obtained for the converter with the following specifications:

- Input voltage is 24 V
- Output voltage swing is 20 V
- The load resistance is 15 Ω
- Frequency of the modulated sine wave is 200 kHz

The transistor that was analyzed was EPC1015 GaN HEMT. Analyzing the curve in Figure 6, it can be seen that for A approximately equal to 1.4, efficiency has the highest value, i. e. this point corresponds to the optimum efficiency point.

If the value for R_{LOAD} is changed to 6Ω, with the same specifications regarding the input voltage, output voltage and frequency of the modulated sine wave, the efficiency dependence is different (Figure 7) and the optimum point is shifted to the lower value of A and higher switching frequency. In a similar manner, if the R_{LOAD} is changed to the higher values, the optimum point is shifted to the higher values of A and lower switching frequency.

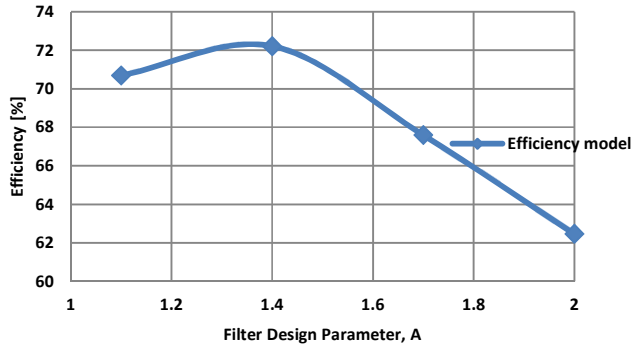

Fig. 6. Efficiency model for different filter designs for R=15Ω

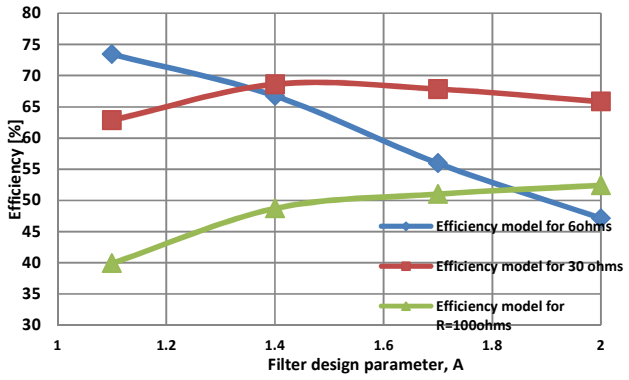

Fig. 7. Efficiency model for different filter designs for R=6Ω, 30Ω and 100Ω

III. COMPARISON OF GALLIUM NITRIDE AND SILICONE DEVICES

New generation of GaN devices is very promising for high voltage, high temperature and high switching frequency applications, because of their superior conductivity and switching characteristics over Si devices. In the aim of reduction of power losses at high switching frequencies, GaN HEMTs present a good choice for Synchronous Buck in RF application [10]. In order to make the comparison between different devices for the same specifications, we use the Figure of Merit which is defined as

$$FOM = Q_G * R_{DS\,ON} \quad (16)$$

For the same specifications regarding the breakdown voltage and maximum drain current, FOMs for GaN HEMT from EPC and two Si MOSFETs from Infineon [11] are presented in Table 1. These Si devices were selected because of their good value for the FOM. Still, it can be seen that EPC1015 has much better FOM than BSC016N04LSG and BSZ097N04LSG, at least for a certain range of frequencies, voltages and power.

Device	Type	V_{ds_max}[V]	R_{on}[mΩ]	Q_G[nC]	FOM
EPC1015	**GaN**	**40**	**3.2**	**11.6**	**37.1**
BSZ097N04LSG	**Si**	**40**	**11.4**	**8.6**	**98.04**
BSC016N04LSG	**Si**	**40**	**1.8**	**54**	**97.2**

Table 1. Characteristics of the devices

IV. EXPERIMENTAL RESULTS

In order to verify the aforementioned theory and to make the experimental comparison of GaN and Si devices, three prototypes were made.

The first prototype was made using two EPC1015 GaN HEMTs, two isolation chips ISO721 and two EL7155 drivers, while a XILINXs SPARTAN3 FPGA board was used to provide the control signals. The simplified schematic of the topology is presented in Figure 8.

In order to make a comparison with Si MOSFETs, the second and the third prototypes were built using BSZ097N04LSG and BSC016N04LSG Si power transistors from Infineon [11], with previously calculated values for FOM. All of the three prototypes were made the same, regarding the PCB layout, isolation chips and drivers that were used, in order to make the precise comparison between the performance of GaN and Si devices. The only difference in the PCB layout was the footprint for the switching devices.

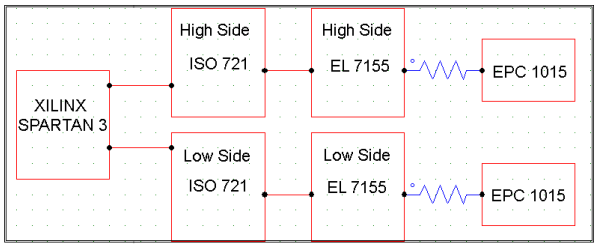

Fig. 8. Simplified schematic of a driving circuit with GaN HEMTs

The drain-to-source voltage waveform of the low-side switch, in the case of both Si MOSFETs showed higher overshoot comparing to the GaN HEMT (Fig. 9 and 10), due to higher leakage inductance of PG-TSDSON-8 Si transistor package. This fact limits the value of the input voltage that can be applied to the Si prototypes. In order to apply 24V at the input of each prototype, it was necessary to put additional resistance in the gate of a high-side Si MOSFETs in order to obtain slower turn-on of a high-side switch and a lower overshoot. Measurements showed that in the case of BSC016N04LSG it was enough to add 1.5Ω in the gate while in the case of BSZ097N04LSG, 3.3 Ω was added in order to achieve safe operating conditions with 24V at the input.

A. Static characteristics

The first efficiency measurements for each prototype were made for a constant output power, at switching frequency equal to 4.7MHz, changing the value for the duty cycle in order to provide different power levels at the output. For input voltage equal to 24V and output resistance of 6Ω, duty cycle was changed from 30% to 70%. The efficiency measurements were made in this manner because in RF application, the output voltage of the converter tracks the RF reference by the modulation of the duty cycle, while the load resistance is being constant.

The efficiency measurements for all three prototypes are presented in Figure 11. The prototype with GaNs showed higher efficiency in the low power range, which is the goal in the case of Envelope Amplifier, because of the high peak-to-average power ratio (PAPR) of the transmitted signals, such as WCDMA.

B. Dynamic test

Next, 64QAM signal with 1MHz of bandwidth was generated. Applied input voltage was equal to 24V and switching frequency was set to 4.7MHz. In order to measure the efficiency in lower and higher power range (around 14W and 31W), output resistance was set to 15Ω and 6Ω, respectively. The obtained results are presented in Table 2 and 3. The measured efficiency included driving losses.

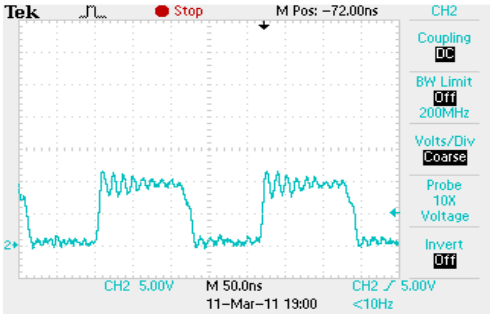

Fig. 9. Measured Vds of the low-side switch in GaN prototype for Vin=10V

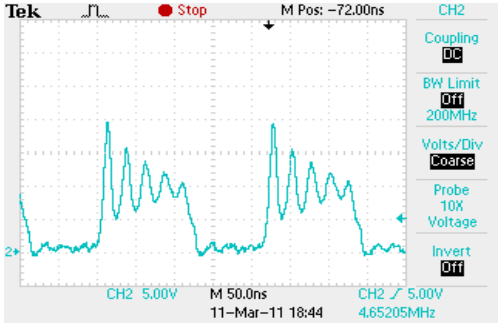

Fig. 10. Measured Vds of the low-side switch in prototype with BSZ097N04LSG MOSFETs for Vin=10V

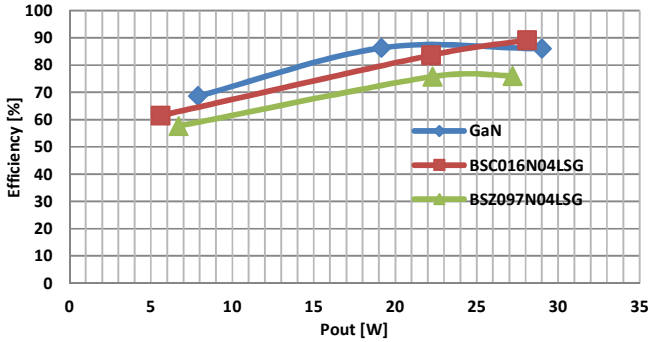

Fig. 11. Efficiency measurement for all three prototypes at 4.7MHz for R_{LOAD} =6 Ω

	GaN	BSC016N04LSG	BSZ097N04LSG
$P_{out,avg}$[W]	**14.4**	**14.2**	**13.8**
Eff [%]	**79.2**	**74.7**	**67.3**

Table 2: Obtained results for 64QAM and R=15Ω

	GaN	BSC016N04LSG	BSZ097N04LSG
$P_{out,avg}$[W]	**31.3**	**31.9**	**30.8**
Eff [%]	**85.9**	**92.2**	**75.3**

Table 3: Obtained results for 64QAM and R=6Ω

The obtained results for average output power around 14W showed higher efficiency of a GaN prototype comparing to the both Si prototypes: 4.5% comparing with the prototype with BSC016N04LSG and 11.9% comparing with the one with BSZ097N04LSG. In the case of $P_{OUT,AVG}$ around 31W,

Si prototype with BSC016N04LSG showed the highest efficiency, as it was expected from the efficiency curves presented in Figure 11.

After 64QAM, Wideband Code Division Multiple Access (WCDMA) sequence was generated and presented in Figure 12. With switching frequency equal to 5MHz, input voltage of 24V and output resistance of 6Ω, envelope with the bandwidth of 500kHz was generated. Obtained results are presented in Table 4. Prototype with GaN showed 3% higher efficiency comparing to the prototype with BSC016N04LSG and 11.5% higher efficiency, comparing to the one with BSZ097N04LSG.

	GaN	BSC016N04LSG	BSZ097N04LSG
$P_{out,\,avg}$[W]	16.3	16.1	15.8
Eff [%]	79.8	76.8	68.3

Table 4: Obtained results for R=6Ω

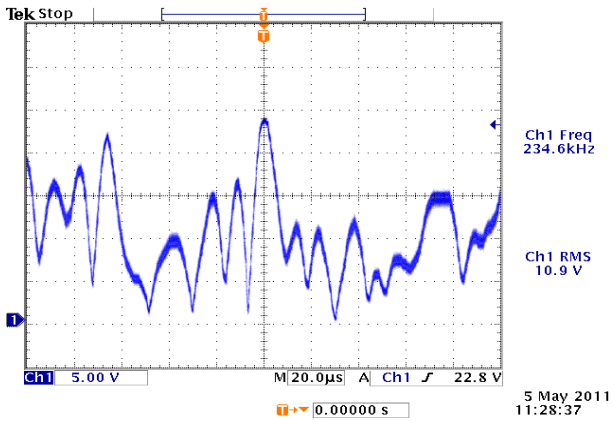

Fig. 12. Generated WCDMA signal with GaN prototype

Regarding the filter design methodology, four filter designs were made, for four different values of paremeter A. For V_{IN}=24V and R_{LOAD}=15Ω, sinusoidal output voltage of 200kHz with the voltage swing of 21V was generated, using the prototype with GaN HEMTs. Obtained results are presented in Table 5. As it was previously mentioned, lower A values correspond to higher switching lossess and higher A values to higher conduction losses. Experimental results showed good correspondence with the power losses model, regarding the determination of the efficiency optimum point (Figure 13) which is found for A around 1.4. Still, there is an offset between the predicted and obtained efficiency values, which demands an improvement of the losses model. For A=1.4, output voltage waveform is presented in Figure 14.

V. CONCLUSIONS AND FUTURE WORK

Design of an Envelope Amplifier using new switching devices based on Gallium Nitride and filter design methodology for this application, were proposed in this paper. Regarding the filter design, power losses dependence on the filter design parameter A in the case of sinusoidal output voltage was derived and the efficiency optimum point was found. Experimental results showed good correspondence with the model regarding the determination of the optimum efficiency point and verified the proposed methodology.

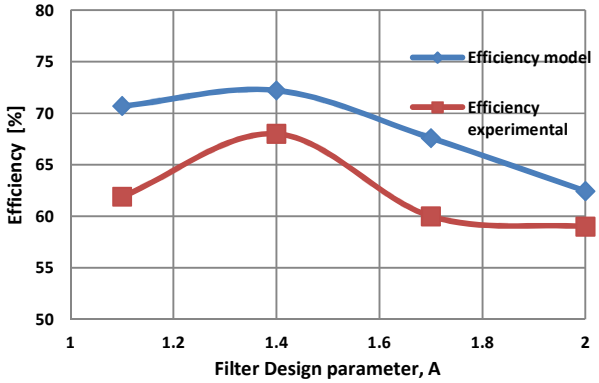

Fig. 13. Comparison of efficiency model and experimental results for different filter designs, for R=15Ω

	A = 1.1	A =1.4	A = 1.7	A = 2.0
f_{SW}[MH_Z]	5.9	4.2	3.7	3.5
L[uH]	8.7	8.9	8.1	7.4
C[nC]	18	40	56	66
P_{LOSSES}[W]	5.6	4.9	6.9	8.3

Table 5. Comparison of four different filter designs for the average output power of 10W

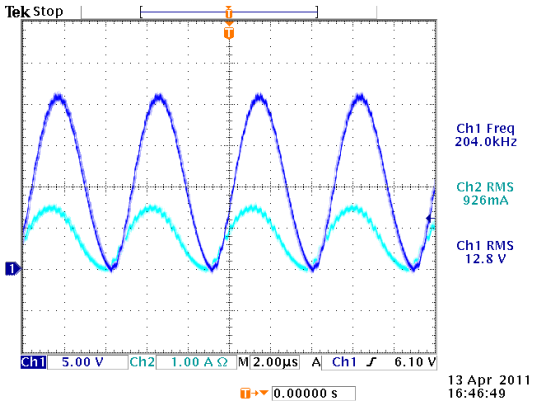

Fig. 14. Sinusoidal output voltage (dark blue) and inductor current (light blue) for A=1.4

On the other hand, comparing with two fast switching Si MOSFETs with good Figure Of Merit, application of GaN

HEMTs showed higher efficiency for 64QAM and WCDMA signals with the average output power around 14W and 16W, respectively.

Regarding the future work, comparison between the different switching devices (Si and GaN transistors) and their performance should be done more precisely. The devices should be selected not only by the Figure Of Merit value, but should have similar values of on-resistance and gate charge as well.

Speaking of filter design, it is necessary to generalize the methodology for random signals such as WCDMA, in order to apply the proposed methodology in a RF transmitter.

Also, in order to increase the bandwidth of the transmitted signal, it is necessary to increase the switching frequency of the converter. One of the main chalenges in that process are requirements for the driver, regarding the current capability and speed. Also, power losses model for GaN HEMTs needs to be derived, in order to make an improvement of the existing model dependence on the filter design parameter.

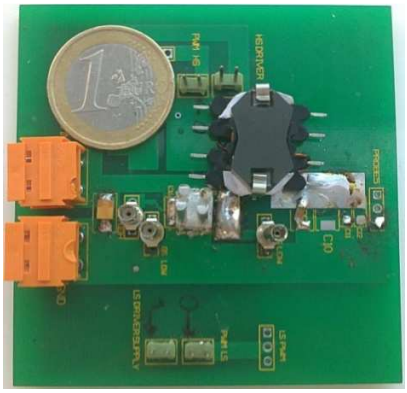

Fig. 15. Prototype with GaN HEMTs

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